ABSTRACT OF THE DISCLOSURE

[[According to one aspect of the present invention, a system including a pipeline microprocessor for out-of-order processing of predicated instructions is disclosed. The microprocessor includes multiple dynamic pipeline stages including at least one predicated instruction wherein the predicated instruction includes at least one guarding predicate. The microprocessor also includes a register renaming unit, a reorder buffer, multiple execution units and multiple reservation stations. The register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the dynamic pipeline stages. The microprocessor also includes an augmented register alias table. Also disclosed is a method of operating a microprocessor for out-of-order processing of predicated instructions.]]

--A method and apparatus for deferring renaming of an instruction that consumes a destination defined by one of a multiple predicated instructions. In one embodiment of the invention, an instruction renaming is deferred by injecting of one or more micro-operations ("uops") into a list of uops to be executed.--.